a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

12. (Amended) A vertical capacitor, comprising:

a bottom electrode;

a top electrode positioned above the bottom electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

16. (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the metal in the buffer layer is a refractory metal.

20. (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the bottom electrode comprises a metal nitride having a metal component which is the same as the metal component of the metal oxide buffer layer.

23.(Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

25.(Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, tantalum oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode is selected from the group consisting of the bottom electrode and the top electrode includes tungsten nitride.

26.(Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer has an orthorhomic crystal structure.

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28. (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

30. (Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes;

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

73.(Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

74. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

75. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein at least one electrode selected from the group consisting of the first electrode and the second electrode comprises tungsten nitride.

76. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

77. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a high temperature annealed, tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

79. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode

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and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has an orthorhomic crystal lattice structure.

80. (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

81. (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

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a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

83. (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

84. (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode

and the second electrode, wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

85.(Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

86. (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

87. (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed, metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

88. (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

90.(Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

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a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

91. (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the

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first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit

wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride.

92. (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a <u>single compound,</u> dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

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a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

93. (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

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94. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

96. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

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a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

97. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having

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an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

98. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

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99. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

100. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of

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integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

102. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

103. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has an orthorhomic crystalline structure.

104. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

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a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer.

105. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

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106. (Amended) A capacitor, comprising:

an annealed bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

110. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

113. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

116. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

118. (Amended) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

124. (Amended) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

125. The memory cell according to claim 124, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.